UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/037,436	12/31/2001	James M. Dodd	5038-184	4824

7590 05/18/2004

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW MORRISON STREET
PORTLAND, OR 97205

EXAMINER	
DANG, KHANH NMN	
ART UNIT	**PAPER NUMBER**
2111	4

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,436	DODD ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,9,12-26,29 and 30* is/are rejected.

7)☒ Claim(s) *2,3,6,8,10,11,27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 15, 16, 19-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 15, "the memory" (line 16) lacks antecedent basis.

In claim 19, the term "approximate state" is unclear and cannot be ascertained.

In claim 20, "the state" lacks clear antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by the acknowledged prior art of Figs. 2 (Prior Art).

As broadly drafted, these claims do not define any structure that differs from the prior art.

The prior art discloses a memory controller (42) comprising: an address/command generator to generate address and command signals (on address/command bus 28) for multiple memory units (46A/46B), including READ command signals, wherein the READ command signals identify the memory unit currently being addressed. It is clear that the READ command signal identify the memory unit because the "[a]ddress signals specify the location within a memory device where data is to be read from". See at least page 1, lines 22-23, of the originally filed specification.

Claims 15-19, 24, 29, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by the Klein.

At the outset, it is noted that it has been held that the recitation that an element is "capable of" performing a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. In re Hutchison, 69 USPQ 138.

As broadly drafted, these claims do not define any structure that differs from the prior art.

With regard to claim 15, Klein discloses a memory controller (22/23) comprising: an address/command generator to generate address and command signals (on address bus 66/command bus 68) for multiple memory units (memory modules 60 or memory modules 76, for example), including READ command signals, wherein the READ command signals identify the memory unit currently being addressed. It is clear that the

READ command signal can identify the memory unit because the location of memory device has already been specified by the address signals.

With regard to claim 16, see at least Fig. 6 and description thereof.

With regard to claim 17, Klein discloses a method of operating a memory device (60/76) comprising: terminating an external data bus on the memory device with a controllable line termination circuit (including transfer gates 64) having on and off states; monitoring the state of the memory device (to monitor whether the memory device is selected for READ or WRITE operations); and setting the state of the line termination circuit based on the state of the memory device (the memory device is selected).

With regard to claim 18, the line termination parameters (states) are stored in a decoder registers (decoder includes registers for storing instruction to be decoded), wherein setting the state of the line termination circuit is further based on the state of the parameters (the decoded states).

With regard to claim 19, as best the Examiner can ascertain from the language of the claim, the decoded read and write commands are received from an external memory controller (22/23), even when the memory device is not selected for reading or writing by the controller (In Klein, in a system of several memory modules, a state decoder is provided for each module, and a different gate control signal will be routed to each module); and interpreting from the decoded commands the approximate state of the data bus; wherein setting the state of the line termination circuit is further based on the approximate state of the data bus (whether read or write is performed on the data bus).

With regard to claim 24, it is clear that in Klein, the "parameters" include the OFF or CLOSE state for turning-off the transfer gates.

With regard to claim 29, Klein discloses an article of manufacture containing computer instructions that, when executed by a processor, perform a method comprising transferring a register value (bits) to a termination parameter register (it is inherent that the state decoder includes registers for storing instruction to be decoded) in a memory unit (memory modules 60 or memory modules 76, for example) served by a data bus (70), the register value (bits) including fields (it is clear that the control bits from control bus 68 includes bits for indicating the state condition for the state decoder) to indicate, to the memory unit, state conditions under which the memory unit should enable and/or disable a data bus line termination circuit (including transfer gates 64) on the memory unit.

With regard to claim 30, see column 5, lines 18-40; column 5, line 5 to column 6, line 7.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 5, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein in view of the acknowledged prior art of Fig. 2.

At the outset, it is noted that similar claims will be grouped together to avoid repetition. It is also noted that it has been held that the recitation that an element is "capable of" performing a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. In re Hutchison, 69 USPQ 138.

With regard to claims 1 and 25, Klein discloses a memory system comprising: an address bus (66)/control and command bus (68); a multidrop data bus (70) having a predetermined number of data signaling lines; a memory controller (22/23) to transmit address and command signals on the address bus (66)/control or command bus (68), and to transmit and receive data signals on the multidrop data bus (70) corresponding to the address and command signals; and first and second memory units (memory modules 60 or memory modules 76), each connected to both the address/command bus and the multidrop data bus, at least the second memory unit (at least one of the memory modules 60 or memory modules 76) comprising controllable termination circuitry (including transfer gate 64) having on and off states and coupled to the multidrop data bus (70), and termination control logic (programmable logic)) to set the state of the termination circuitry according to decoded commands (decoded by state decoder 78, for example) received on the control/command bus (68). With regard to claim 4, it is clearly inherent that the state decoder includes registers for storing instruction to be decoded in memory modules 60 or memory modules 76, for example. It is also clear that the control bits from control bus 68 includes bits for indicating the state condition for the state decoder. With regard to claim 5, in Klein, the memory system

supports different types of memory configuration, and the memory controller can be configured accordingly. See column 5, lines 18-40; column 5, line 5 to column 6, line 7. With regard to claim 26, in Klein, the memory units can be different. Thus, their internal parameters are different, and therefore the state is set depending on the internal parameters. See column 5, lines 18-40; column 5, line 5 to column 6, line 7.

Klein does not disclose that address signals and control/command signals may share the same bus. However, the prior art disclose that address/command bus "may have separate address lines and command lines [as in Klein], or addresses and commands may share a common set of lines and use temporal address/command separation." See page 2, lines 1-3 of the originally filed specification.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a common bus for both address signals and control/command signals, as taught by the prior art, for the purpose of cost saving, or because such a modification is merely a design choice and involves only routine skill in the art.

Claims 9, 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein in view of the acknowledged prior art of Fig. 2.

At the outset, it is noted that similar claims will be grouped together to avoid repetition. It is also noted that it has been held that the recitation that an element is "capable of" performing a function is not a positive limitation but only requires the ability

to so perform. It does not constitute a limitation in any patentable sense. In re Hutchison, 69 USPQ 138.

With regard to claim 9, Klein discloses a memory device (60/76) comprising: a memory cell array (62); a bi-directional data port (it is clear that bi-directional data bus 70 must have data port) capable of receiving data for and transmitting data stored in the memory cell array (62); an address bus 66 (it is clear that address bus must have address port) and command bus 68 (it is clear that command bus must have command port); a controllable line termination circuit (including transfer gates 64) to terminate signals at the data port (of data bus 70), the circuit having on and off states (open/close); an address and command decoder (state decoder 78, for example) to receive signals; and termination control logic (programmable logic) coupled to the address and command decoder to set the state of the termination circuitry according to decoded commands from the decoder. With regard to claim 12, it is inherent that the state decoder includes registers for storing instruction to be decoded. With regard to claim 13, it is clear that in Klein, the "parameters" include the OFF or CLOSE state for turning-off the transfer gates. With regard to claim 14, see discussion regarding claims 17 and 18.

Klein does not disclose that address signals and control/command signals may share the same bus. However, the prior art disclose that address/command bus "may have separate address lines and command lines [as in Klein], or addresses and commands may share a common set of lines and use temporal address/command separation." See page 2, lines 1-3 of the originally filed specification.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a common bus for both address signals and control/command signals, as taught by the prior art, for the purpose of cost saving, or because such a modification is merely a design choice and involves only routine skill in the art.

Allowable Subject Matter

Claims 2, 3, 6-8, 10, 11, 27, and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 20-23 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

U.S. Patent Nos. 5,604,714 to Manning et al., 6,304,502 to Watanabe et al., and 6,496,945 to Cepulis are cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner